

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-7. (Canceled)

8. (Currently Amended) A method of manufacturing a circuit comprising:
forming first and second semiconductor layers over a substrate;
forming a gate insulating film over the first and the second semiconductor layers;
forming gate electrodes over the first and the second semiconductor layers with the gate insulating film interposed therebetween;

introducing a first impurity element into portions of the first and the second semiconductor layers so as to form a pair of first impurity regions with a channel formation region interposed therebetween;

introducing a second impurity element into portions of the first and the second semiconductor layers so as to form a pair of second impurity regions ~~in contact~~ with the pair of first impurity regions interposed therebetween; and

introducing a third impurity element into portions of the first semiconductor layer so as to form a pair of third impurity regions ~~in contact~~ with the pair of second impurity regions interposed therebetween,

wherein an edge of the gate insulating film is aligned with a boundary between the pair of second impurity regions and the pair of third impurity regions.

9. (Currently Amended) A method of manufacturing a circuit according to claim 8 wherein a concentration of the pair of third impurity regions is higher than that of the

pair of second impurity regions, and a concentration of the pair of second impurity regions is higher than that of the pair of first impurity regions.

10. (Previously Presented) A method of manufacturing a circuit according to claim 8 wherein the first, the second, and the third impurity elements comprise phosphorus.

11. (Previously Presented) A method of manufacturing a circuit according to claim 8 wherein the circuit is a logic circuit.

12. (Previously Presented) A method of manufacturing a circuit according to claim 8 wherein the circuit is incorporated in an electroluminescence display device.

13. (Previously Presented) A method of manufacturing a circuit according to claim 8 wherein the circuit is incorporated in at least one selected from the group consisting of a cellular phone, a video camera, a mobile computer, a goggle-type display, a projector, and an electronic book.

14. (Currently Amended) A method of manufacturing a circuit comprising:
forming first and second semiconductor layers over a substrate, wherein the first semiconductor layer has a larger width than that of the second semiconductor layer;
forming a gate insulating film over the first and the second semiconductor layers;
forming gate electrodes over the first and the second semiconductor layers with the gate insulating film interposed therebetween;
introducing a first impurity element into portions of the first and the second semiconductor layers so as to form a pair of first impurity regions with a channel formation region interposed therebetween;

introducing a second impurity element into portions of the first and the second semiconductor layers so as to form a pair of second impurity regions ~~in contact~~ with the pair of first impurity regions interposed therebetween; and

introducing a third impurity element into portions of the first semiconductor layer so as to form a pair of third impurity regions ~~in contact~~ with the pair of second impurity regions interposed therebetween.

15. (Currently Amended) A method of manufacturing a circuit according to claim 14 wherein a concentration of the pair of third impurity regions is higher than that of the pair of second impurity regions, and a concentration of the pair of second impurity regions is higher than that of the pair of first impurity regions.

16. (Previously Presented) A method of manufacturing a circuit according to claim 14 wherein the first, the second, and the third impurity elements comprise phosphorus.

17. (Previously Presented) A method of manufacturing a circuit according to claim 14 wherein the circuit is a logic circuit.

18. (Previously Presented) A method of manufacturing a circuit according to claim 14 wherein the circuit is incorporated in an electroluminescence display device.

19. (Previously Presented) A method of manufacturing a circuit according to claim 14 wherein the circuit is incorporated in at least one selected from the group consisting of a cellular phone, a video camera, a mobile computer, a goggle-type display, a projector, and an electronic book.

20. (Currently Amended) A method of manufacturing a circuit comprising:

forming first and second semiconductor layers over a substrate;
forming a gate insulating film over the first and the second semiconductor layers;
forming gate electrodes over the first and the second semiconductor layers with the gate insulating film interposed therebetween;
introducing a first impurity element into portions of the first and the second semiconductor layers so as to form a pair of first impurity regions with a channel formation region interposed therebetween;
introducing a second impurity element into portions of the first and the second semiconductor layers so as to form a pair of second impurity regions ~~in contact~~ with the pair of first impurity regions interposed therebetween;
introducing a third impurity element into portions of the first semiconductor layer so as to form a pair of third impurity regions ~~in contact~~ with the pair of second impurity regions interposed therebetween; and
forming wirings so as to be in contact with the pair of third impurity regions,
wherein an edge of the gate insulating film is aligned with a boundary between the pair of second impurity regions and the pair of third impurity regions.

21. (Currently Amended) A method of manufacturing a circuit according to claim 20 wherein a concentration of the pair of third impurity regions is higher than that of the pair of second impurity regions, and a concentration of the pair of second impurity regions is higher than that of the pair of first impurity regions.

22. (Previously Presented) A method of manufacturing a circuit according to claim 20 wherein the first, the second, and the third impurity elements comprise phosphorus.

23. (Previously Presented) A method of manufacturing a circuit according to claim 20 wherein the circuit is a logic circuit.

24. (Previously Presented) A method of manufacturing a circuit according to claim 20 wherein the circuit is incorporated in an electroluminescence display device.

25. (Previously Presented) A method of manufacturing a circuit according to claim 20 wherein the circuit is incorporated in at least one selected from the group consisting of a cellular phone, a video camera, a mobile computer, a goggle-type display, a projector, and an electronic book.

26. (Currently Amended) A method of manufacturing a circuit comprising:
forming first and second semiconductor layers over a substrate, wherein the first semiconductor layer has a larger width than that of the second semiconductor layer;
forming a gate insulating film over the first and the second semiconductor layers;
forming gate electrodes over the first and the second semiconductor layers with the gate insulating film interposed therebetween;
introducing a first impurity element into portions of the first and the second semiconductor layers so as to form a pair of first impurity regions with a channel formation region interposed therebetween;
introducing a second impurity element into portions of the first and the second semiconductor layers so as to form a pair of second impurity regions ~~in contact~~ with the pair of first impurity regions interposed therebetween;
introducing a third impurity element into portions of the first semiconductor layer so as to form a pair of third impurity regions ~~in contact~~ with the pair of second impurity regions interposed therebetween; and
forming wirings so as to be in contact with the pair of third impurity regions.

27. (Currently Amended) A method of manufacturing a circuit according to claim 26 wherein a concentration of the pair of third impurity regions is higher than that of the

pair of second impurity regions, and a concentration of the pair of second impurity regions is higher than that of the pair of first impurity regions.

28. (Previously Presented) A method of manufacturing a circuit according to claim 26 wherein the first, the second, and the third impurity elements comprise phosphorus.

29. (Previously Presented) A method of manufacturing a circuit according to claim 26 wherein the circuit is a logic circuit.

30. (Previously Presented) A method of manufacturing a circuit according to claim 26 wherein the circuit is incorporated in an electroluminescence display device.

31. (Previously Presented) A method of manufacturing a circuit according to claim 26 wherein the circuit is incorporated in at least one selected from the group consisting of a cellular phone, a video camera, a mobile computer, a goggle-type display, a projector, and an electronic book.

32. (Currently Amended) A method of manufacturing a circuit comprising:
forming first and second semiconductor layers over a substrate, wherein the first semiconductor layer has a larger width than that of the second semiconductor layer;
forming a gate insulating film over the first and the second semiconductor layers;
forming gate electrodes over the first and the second semiconductor layers with the gate insulating film interposed therebetween;
introducing a first impurity element into portions of the first and the second semiconductor layers so as to form a pair of first impurity regions with a channel formation region interposed therebetween;

introducing a second impurity element into portions of the first and the second semiconductor layers so as to form a pair of second impurity regions ~~in contact~~ with the pair of first impurity regions interposed therebetween;

introducing a third impurity element into portions of the first semiconductor layer so as to form a pair of third impurity regions ~~in contact~~ with the pair of second impurity regions interposed therebetween; and

forming wirings so as to be in contact with the pair of third impurity regions,

wherein an edge of the gate insulating film is aligned with a boundary between the pair of second impurity regions and the pair of third impurity regions.

33. (Currently Amended) A method of manufacturing a circuit according to claim 32 wherein a concentration of the pair of third impurity regions is higher than that of the pair of second impurity regions, and a concentration of the pair of second impurity regions is higher than that of the pair of first impurity regions.

34. (Previously Presented) A method of manufacturing a circuit according to claim 32 wherein the first, the second, and the third impurity elements comprise phosphorus.

35. (Previously Presented) A method of manufacturing a circuit according to claim 32 wherein the circuit is a logic circuit.

36. (Previously Presented) A method of manufacturing a circuit according to claim 32 wherein the circuit is incorporated in an electroluminescence display device.

37. (Previously Presented) A method of manufacturing a circuit according to claim 32 wherein the circuit is incorporated in at least one selected from the group

consisting of a cellular phone, a video camera, a mobile computer, a goggle-type display, a projector, and an electronic book.